REMARKS

Applicant would like to thank the Examiner for the thorough examination of the present application. Applicant would also like to thank the Examiner for correctly indicating as allowable the subject matter of dependent Claims 20-21, 27-28, 32-33 and 36-37.

The independent claims have been amended to more clearly define the present invention over the cited prior art references. Support in the specification for the claim amendments may be found in paragraph 27, for example. The claim amendments and arguments supporting patentability of the claims are provided below.

I. The Amended Claims

The present invention, as recited in amended independent Claim 15, for example, is directed to a computer system comprising at least one peripheral for generating interrupt requests, an interrupt pending register for storing the interrupt requests, and a microprocessor for processing interrupts. An interrupt control circuit is coupled to the interrupt pending register and the microprocessor for providing an interrupt command to the microprocessor based upon the stored interrupt requests.

An auxiliary interrupt control circuit is coupled to the at least one peripheral and the microprocessor for generating a bit string identifying an active bit stored in the interrupt pending register of the peripheral that generated the interrupt request and which corresponds to a highest priority interrupt request to be processed, and for providing the bit string to the microprocessor.

The microprocessor identifies and processes an interrupt corresponding to the highest priority interrupt request based upon the bit string and the interrupt command without having to perform any external operations. Identification of the interrupt to be served is significantly less burdensome on the microprocessor executing the corresponding routine. This is done by generating in the peripheral a bit string identifying, by a corresponding active bit of the string, the interrupt to be served, and sending this bit string to the microprocessor that will recognize the interrupt and eventually serve it by executing the corresponding routine.

Moreover, by generating a bit string which identifies the position of an active bit in the interrupt pending register of the peripheral requesting the interrupt, and sending the bit-string to the microprocessor, the microprocessor is able to substantially immediately recognize which interrupt of the peripheral is to be served or processed without having to read the interrupt pending register and without having to perform another operation to identify the peripheral that generated the interrupt request.

Independent Claim 23 is directed to an auxiliary interrupt control circuit for use in a computer system, and has been amended similarly to amended independent Claim 15.

Independent Claim 29 is directed to a peripheral to be coupled to a microprocessor, and has been amended similarly to amended independent Claim 15.

Independent Claim 34 is directed to a method for processing peripheral interrupts, and has been amended similarly to amended independent Claim 15.

II. The Claims Are Patentable

The Examiner rejected independent Claims 15, 23, 29 and 34 over the Moyer et al. patent. The Moyer et al. patent is directed to a data processing system **10** that has a multi-field register **62** with two fields: a selection field **90** and an information field **91**. The selection field **90** identifies the source of the information loaded in the information field **91**.

The multi-field register **62** is an interrupt flag register **62** and the selection field **90** identifies which of the two register portions **59**, **60** of the interrupt pending register **58** is loaded into the multi-field register **62**. The low register portion **59** can identify up to thirty-one sources of interrupt requests, and the high register portion **60** can identify up to thirty-two sources of interrupt requests even though the information field **91** is only thirty-one bits. This is achievable because the selection field **90** serves a dual function, namely as a flag bit and as bit-32 of the interrupt pending register **58**. Reference is directed to column 6, lines 9-13 of the Moyer et al. patent, which provides:

> "Thus CPU reads the interrupt flag register **62** and uses the least significant bit **90** to determine whether the rest of the bits of interrupt flag register **62** contain information on interrupt request sources **1-31** or interrupt request sources **32-63**."

The CPU in the Moyer et al. patent recognizes which interrupt is to be served or processed by reading the

interrupt pending register **58** (i.e., via the dual function of the selection field **90**) of the peripheral.

In sharp contrast, amended independent Claim 15 has been amended to recite that the microprocessor identifies an interrupt corresponding to the highest priority interrupt request based upon the bit string and the interrupt command without having to read the interrupt pending register and without having to perform another operation to identify the peripheral that generated the interrupt request. Reference is directed to paragraph 27 from the Applicant's specification, which provides:

> "The bit string identifies the position of an active bit stored in the interrupt pending register of the peripheral that required the interrupt, and it corresponds to the interrupt to be served. This bit string is sent to the microprocessor which knows substantially immediately which interrupt is to be served based thereon. This is so even if the control circuit received an interrupt signal resulting from ORing different interrupt flags. Therefore, the processor need not read the contents of the interrupt pending register of the peripheral that has requested the interrupt. Instead, it may serve it directly." (Emphasis added)

The microprocessor in the claimed invention does not have to read the interrupt pending register and nor does it have to perform another operation to identify the peripheral that generated the interrupt request. The microprocessor is able to make this determination based upon the received bit string. In Moyer et al., the CPU performs another operation by reading the interrupt flag register **62** for determining which interrupt is to be served or processed.

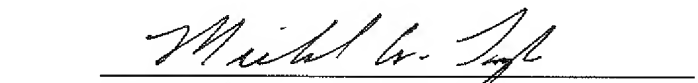
Accordingly, it is submitted that amended independent Claim 15 is patentable over the Moyer et al. patent. Amended independent Claims 23, 29 and 34 are similar to amended independent Claim 15. Therefore, it is submitted that these claims are also patentable over the Moyer et al. patent.

In view of the patentability of amended independent Claims 15, 23, 29 and 34, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

III. CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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